REMARKS

Claims 1-4 were rejected as anticipated by STOLFA et al. 5,965,912. Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 1 includes MOS transistors that are in a substrate and include gate insulating films, and a MOS type varactor element in the substrate and which includes a gate insulating film, where the gate insulating film of the varactor element is thinner than the thinnest gate insulating film among the gate insulating films of the MOS transistors. This is shown, by way of example, in Figures 3A-C that illustrate MOS transistors 1, 2 in Figures 3A-B that have gate insulating films 4 and varactor element 3 in Figure 3C that has a gate insulating film 14 that is thinner than that of the MOS transistors 1, 2.

STOLFA et al. disclose a variable capacitor that includes one MOS transistor with plural fingers. The Official Action states that the MOS transistors are shown in Figure 2 as the elements having gate insulating films 52, 54, 56, and 58, and the indication that the varactor element has a gate insulating film that is thinner than that of the MOS transistors is to be found at column 4, lines 12-14. This citation indicates that the thickness of the gate dielectric layers 52, 54, 56, and 58 determines the maximum capacitance of the capacitor 10 (which includes all the elements having the gate insulating films 52, 54, 56, and 58).

The reference refers at column 4, line 12 to "The thickness of the gate dielectric layers" (emphasis added), clearly implying that these layers have the same thickness.

The reference also states at column 4, lines 22-26 that the steps for forming the dielectric layer, conductive layer and gate structures can be performed in the same steps as those forming the gate structure of a MOSFET (not shown). That is, the gate dielectric layers 52, 54, 56, and 58 can be formed at the same time as the corresponding layers of a MOSFET.

The reference does not state that the gate dielectric layers 52, 54, 56, and 58 formed at the same time as the corresponding layers of a MOSFET are to have a different thickness than those of the MOSFET. The reference indicates that the thickness of the gate insulating film can determine the maximum capacitance of the capacitor, but does not indicate that a different thickness is to be used for the gate insulating layer of the MOSFET, and especially that the varactor gate dielectric layer is to be thinner. Indeed, the reference says that the same steps can be used so one of skill in the art would not add steps that appear to be unnecessary to the manufacturing process. Accordingly, one of skill in the art would not learn from this reference that the gate insulating film of the varactor element is thinner than the thinnest gate insulating film among the gate insulating films of said MOS transistors, as in claim 1 that thereby avoids the rejection under §102.

New claim 5 has been added and is allowable because STOLFA et al. do not disclose the MOS type varactor in the substrate and spaced from the plural MOS transistors, which are not part of a varactor, has a gate insulating film that is thinner than the thinnest gate insulating film among the gate insulating films of the plural MOS transistors.

New claims 6 and 10 are allowable because the reference does not disclose that the gate insulating film of the varactor and the gate insulating films of the MOS transistors are at a same level of the device.

New claims 7 and 11 are allowable because the reference does not disclose that the thickness of the gate insulating film of the varactor is about three quarters of a thickness of the gate insulating films of the MOS transistors.

New claims 8 and 12 are allowable because the reference does not disclose that the thickness of the gate insulating film of the varactor is about 6 nm and the thickness of the gate insulating films of the plural MOS transistors is about 8 nm.

New claims 9 and 13 are allowable because the reference does not disclose that the MOS transistors include an N-channel MOS transistor and a P-channel MOS transistor.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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